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CONFIGURABLE MATRIX ARCHITECTURE

Cross Reference to Related Applications

The present application may relate to co-pending application Serial No. 09/_____, filed August 27, 2001 (Attorney Docket 0325.00502) and Serial No. 09/_____, filed August 29, 2001 (Attorney Docket 0325.00505), which are each hereby incorporated by reference in their entirety.

Field of the Invention

The present invention relates to a method and/or architecture for implementing configurable matrices generally and, more particularly, to a method and/or architecture for implementing multiple configurable matrices having distributed multiplexers and shared input groups.

Background of the Invention

A number of conventional approaches are used to implement multiplexers within configurable matrices. Configurable matrices

implement one or more multiplexers of varying widths. Configurable matrices also have a variable number of inputs and outputs.

Summary of the Invention

The present invention concerns an apparatus comprising a distributed multiplexer configured to receive a distributed input group of signals. The distributed multiplexer may be configured to evenly load the distributed input groups.

The objects, features and advantages of the present invention include providing an architecture and/or method for implementing configurable matrices that may (i) be scalable, (ii) utilize layout area efficiently, (iii) reduce or eliminate the need to re-order matrix inputs, (iv) equalize output routing, (v) allow flexibility of reprogramming multiplexer connections without requiring complete rework of the configurable matrix, and/or (vi) accommodate multiplexers of varying sizes.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram of an embodiment of the present invention; and

FIG. 2 is a detailed block diagram of the circuit of FIG. 1; and

FIG. 3 is a block diagram of another embodiment of the present invention;

FIG. 4 is a detailed block diagram of the circuit of FIG. 3; and

FIG. 5 is a block diagram of an implementation of the present invention.

Detailed Description of the Preferred Embodiments

Referring to FIG. 1, a block diagram of a circuit (or system) 100 is shown in accordance with an embodiment of the present invention. The circuit 100 generally comprises a number of configurable matrices 102a-102n. A configurable matrix may enable

a number of inputs to be routed to a number of outputs and may be referred to as a programmable interconnect matrix (PIM). Each PIM 102a-102n generally comprises a number of multiplexer columns 104a-104n. Each multiplexer column 104a-104n generally comprises a number of multiplexers 106a-106n. The circuit 100 may have inputs (e.g., INPUTS) grouped independently for each of the PIMs 102a-102n (e.g., INA1-INNn). For example, a multiplexer in the PIM 102a may receive the input group INA1, while the multiplexer 106a in the PIM 102n may receive the input group INAn. Each of the PIMs 102a-102n may also comprise an input re-order channel 110. The input re-order channel 110 may be shown as a number of re-order channels 110a-110n for each PIM 102a-102n. The number of PIMs 102a-102n may be different than the number of re-order channels 110. The channels 110a-110n are configured to re-order the input signals for each of the PIMs 102a-102n (e.g., the input re-order channel 110 provides re-ordering for each of the input groups INA1-INAn). For example, the input re-order channel 110a may re-order the input groups INA1-INN1. Additionally, each multiplexer column 104a-104n may have a number of output routes 112a-112n that may present a signal (e.g., OUTPUTS).

Referring to FIG. 2, a detailed schematic of the multiplexer columns 104a-104n and the multiplexers 106a-106n are shown. Each of the multiplexers 106a-106n may comprise n number of multiplexer bits, where n is an integer. For example, the multiplexer 106a may comprise the bits 106a_1-106a_n. Each of the multiplexer bits 106a_1-106n_n may be coupled to the outputs OUTPUTS. The multiplexer bits 106a_1-106n_n may require variable length output routing (e.g., vertical and horizontal routing). Such output routing may introduce variable delay into the circuit 100. The input re-order channels 110a-110n of the PIMs 102a-102n may also cause different loading on the inputs which may increase the propagation delay through the PIMs 102a-102n. Additionally, the width of the PIMs 102a-102n is generally set by the internal input re-ordering channel 110a-110n and/or output routing rather than the area of each PIM 102a-102n.

While the circuit 100 may connect a number of PIMs 102a-102n, the circuit 100 may have (i) non-deterministic parasitic loading on the inputs INPUTS, (ii) different loading parasitics on the outputs OUTPUTS, and (iii) non-deterministic best case and worst case delay paths. Also, layout rework may be required to

reprogram the circuit 100. Furthermore, the circuit 100 is not easily scalable.

Referring to FIG. 3, a block diagram of a circuit (or system) 100' is shown in accordance with another embodiment of the present invention. The circuit 100' may be similar to the circuit 100. However, the circuit 100' may be configured to share input groups across multiple programmable interconnect matrices (PIMs). The circuit 100' may allow input groups to be defined across multiple PIMs. The PIMs may comprise one or more distributed multiplexer circuits. The system 100' may be expanded in either a horizontal or a vertical direction for optimum routability. The system 100' may allow variable multiplexer widths. The system 100' may provide a deterministic (i) layout area and/or (ii) best case and worst case delay path. The system 100' may also be scalable across a family of devices. Furthermore, the system 100' may provide flexible re-programing of multiplexer connections.

Each of the PIMs 102a'-102n' are shown comprising a number of multiplexer columns 104a'-104n'. The particular number of columns 104a'-104n' may be varied in order to meet the design criteria of a particular implementation. Each of the multiplexer

columns 104a'-104n' may comprise a number of multiplexers 106a'-106n' (also labeled MUXA, MUXB, MUXC and MUXD). The multiplexers 106a'-106n' may be implemented as distributed multiplexers. In one example, the multiplexers 106a'-106n' may be implemented as 4:1 multiplexers. However, other appropriate type multiplexers configurations may be implemented accordingly to meet the design criteria of a particular application. Each of the multiplexers 106a'-106n' may comprise n number of bits, where n is an integer. For example, the multiplexer 106a' may comprise the bits 106a_1'-106a_n'. The multiplexer bits 106a_1'-106n_n' may be implemented as PIM bits.

Each of the distributed multiplexers 106a'-106n' may receive a distributed input group (e.g., INA1-INDn). For example, the bit 106a_1' may receive the input group INA1, the bit 106a_2' may receive the input group INA2, the bit 106a_3' may receive the input group INA3, and the bit 106a_n' may receive the input group INAn. The distributed input groups INA, INB, INC and IND may be derived from the signal INPUTS. The distributed input groups INA, INB, INC and IND may be constant across the PIMS 102a'-102n'. The input groups INA, INB, INC and IND may also be constant across the

multiplexer columns 104a'-104n'. The number of input groups may be varied in order to meet the design criteria of a particular implementation. The multiplexers 106a'-106n' of the columns 104a'-104n' may be coupled to the output lines OUTPUTS.

The input signals INPUTS are generally grouped such that the same groups (e.g., INA, INB, INC and IND) may be routed over all of the PIMs 102a'-102n'. Each multiplexer bit generally connects to only one input signal. The input signal groups INA, INB, INC and IND may be routed over the bounding box of the multiplexer bit to which the input signal connects. The PIMs 102a'-102n' may be expanded or contracted according to the number of input routes or multiplexers implemented in the PIM.

Referring to FIG. 4, a detailed diagram illustrating connections of the multiplexers 106a'-106n' is shown. The multiplexer bits 106a_1'-106n_n' may connect the input groups INA, INB, INC and IND and the outputs OUTPUTS. A configuration of the PIMS 102a'-102n' may be expanded or contracted to implement any appropriate number or size of multiplexers. Additionally, the size (e.g., bit width) of the input groups may be varied. The input signals INPUTS may connect to one or more of the PIMs 102a'-102n'.

For example, the bit 106a_1' may receive one of the lines of the group INA1. A bit 107a_1' may receive one of the lines of the group INA1. The line received by the bit 106a_1' may be the same line or a different line than the line received by the bit 107a_1'. Furthermore, a bit 108a_1' may receive one of the lines of the group INA1. The line received by the bit 108a_1' may be the same line or a different line than the line received by the bit 106a_1' and/or the line received by the bit 107a_1'. Each of the multiplexers 106a'-106n' may have only one of the multiplexer bits programmed to allow the signals of the input groups INA, INB, INC, and IND of the signal INPUTS to pass through. The multiplexer output signals OUTPUTS may be connected to a next stage of the PIMs 102a'-102n', which may be another multiplexer stage, output drivers or other appropriate device.

Referring to FIG. 5, a circuit (or system) 200 is shown illustrating an implementation of the present invention. The circuit 200 generally comprises a number of PIMs 202a-202n. The PIMs 202a-202n may be similar to the circuits 102 and/or 102' of the present invention. The particular number of the PIMS 202a-202n may be varied in order to meet the design criteria of a particular

application. Each of the PIMs 202a-202n may receive an input (e.g. INPUTS). The signal INPUTS may comprise multi-bit and/or single-bit signals. In one example, the signal INPUTS may be implemented as a multi-bit input bus. In another example, the signal INPUTS may be implemented as one or more distributed input groups. Each of the PIMs 202a-202n may also be configured to generate an output signal (e.g. OUTPUTS). The signal OUTPUTS may comprise multi-bit and/or single-bit signals. The PIMs 202a-202n may each be implemented as a variable number of multiplexers. A width of the multiplexers may also be varied. For example, the PIM 202a may be implemented as a single multiplexer, two multiplexers, one hundred multiplexers, etc. of variable width. However, the particular number of multiplexers may be varied in order to meet the design criteria of a particular implementation.

The circuit 100 (or 100') may be designed using 0.18µm process technology. However, the present invention may be applicable for other technologies and devices. The present invention may provide a flexible implementation of a programmable interconnect matrix comprising distributed multiplexers and distributed input groups across multiple PIMs. The present

invention may, therefore, reduce or eliminate channel re-ordering, output routing and/or loading. The multiplexer bits may also be in an interleaved (or distributed) configuration. The input signal groupings and sizes of the PIMs 102a'-102n' may be determined across an entire family of devices. The layout area of the present invention may be determined by the size of the multiplexers implemented and not by the interconnect routing. Therefore, a size and/or configuration of the PIMs 102a'-102n' may be deterministic.

The present invention may minimize input parasitic loading by implementing a single short route across a PIM bit. The present invention may also provide similar output loading on all the multiplexers A, B, C and D. The layout area of the PIMs 102a'-102n' to be defined by multiplexer area and not the re-ordering interconnect. The present invention may provide for ease of reprogramming (e.g., contact programmable).

The present invention may allow expansion or contraction of the PIMs in either a horizontal or vertical direction to improve routability. The present invention may produce a deterministic layout area. The present invention may produce a deterministic best case and worst case path delay. The present invention may

provide an input grouping configuration that may allow the inputs to be consistent across multiple PIMs resulting in deterministic delays.

The present invention may allow PIM structure definitions for an entire family of devices. The present invention may allow utilization of the same input groups for the PIMs 102a'-102n'. The present invention may provide a group and/or output routing method. The present invention may provide PIMs with deterministic delays. Such a configuration may allow for rerouting of signals through a PIM without changing the best case or worst case delays through the PIM.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.